FIG.1

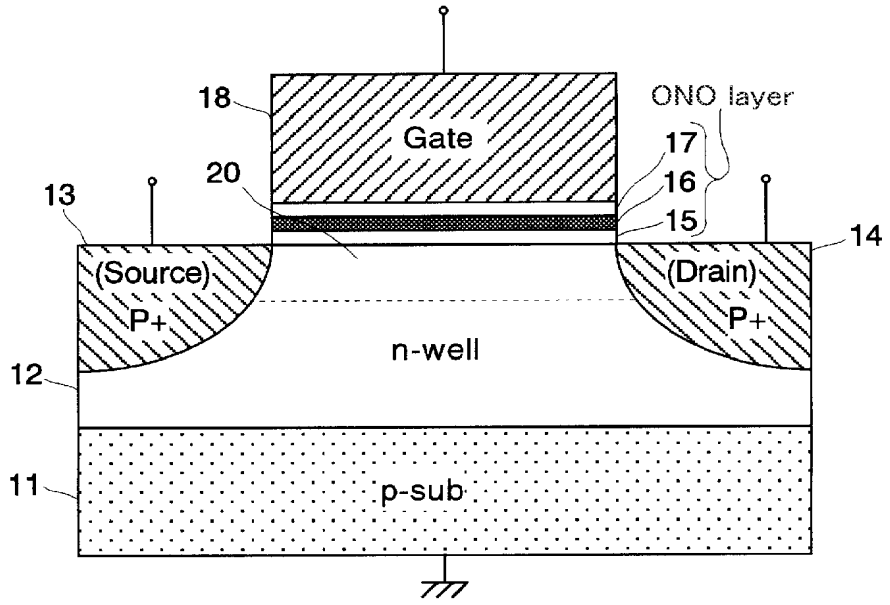
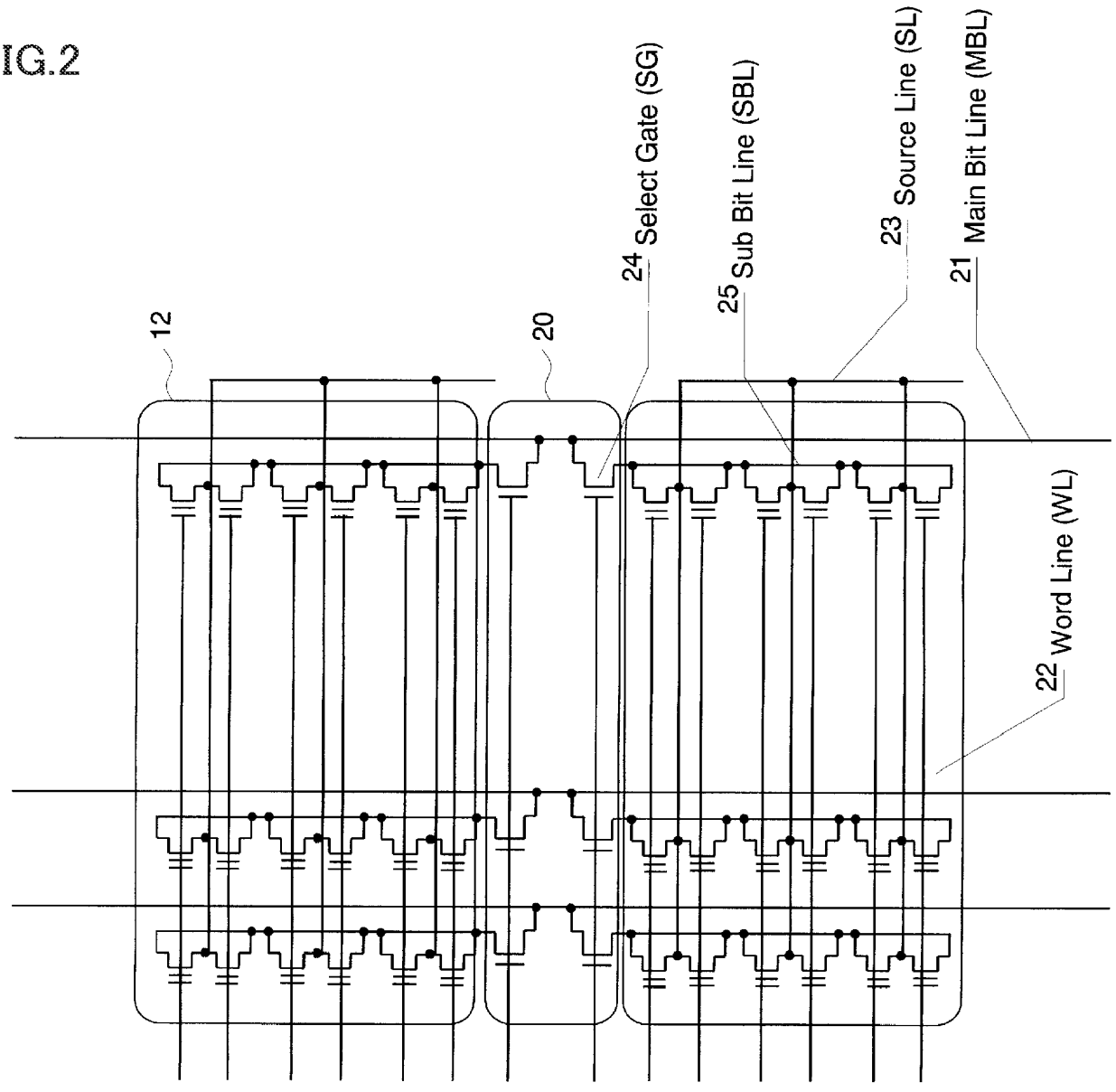

18
Gate
ONO layer
17
16
15
20
13
14
(Source)
P+
(Drain)
P+
n-well
12
11
p-sub

FIG.2


12
20
24 Select Gate (SG)
25 Sub Bit Line (SBL)
23 Source Line (SL)
21 Main Bit Line (MBL)
22 Word Line (WL)

		Program	Prg-verify	Erase(tn)	Erase(hh)	Read
selected	Main-BL	GND	VCC	VCC	VCC	GND
	SG	-2.2V	-2.2V	VCC	VCC	-2.2V
	Sub-BL	GND	VCC	open	open	GND
	WL	10V	-5V	-13V	-13V	-2.2V
	Source	VCC	GND	VCC	-4V	VCC
	Cell-well	4V	4V	VCC	-1V	VCC
	SG-well	VCC	VCC	VCC	VCC	VCC
Un-selected	Main-BL	VCC	VCC	VCC	VCC	VCC
	SG	VCC	VCC	VCC	VCC	VCC
	Sub-BL	open	open	open	open	open
	WL	VCC	VCC	VCC	VCC	VCC
	Source	VCC	VCC	VCC	VCC	VCC
	Cell-well	VCC	VCC	VCC	VCC	VCC
	SG-well	VCC	VCC	VCC	VCC	VCC
sub		GND	GND	GND	GND	GND

FIG.3

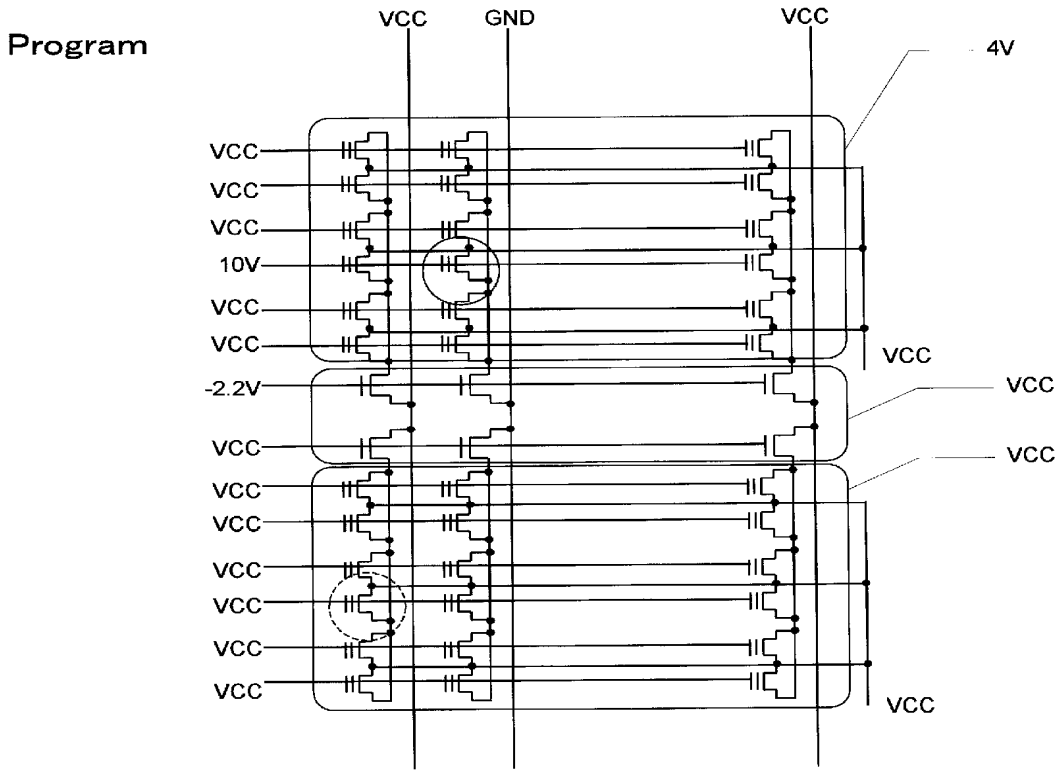

Program
VCC
GND
VCC
4V
VCC
VCC
VCC
10V
VCC
VCC
-2.2V
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC

FIG.4

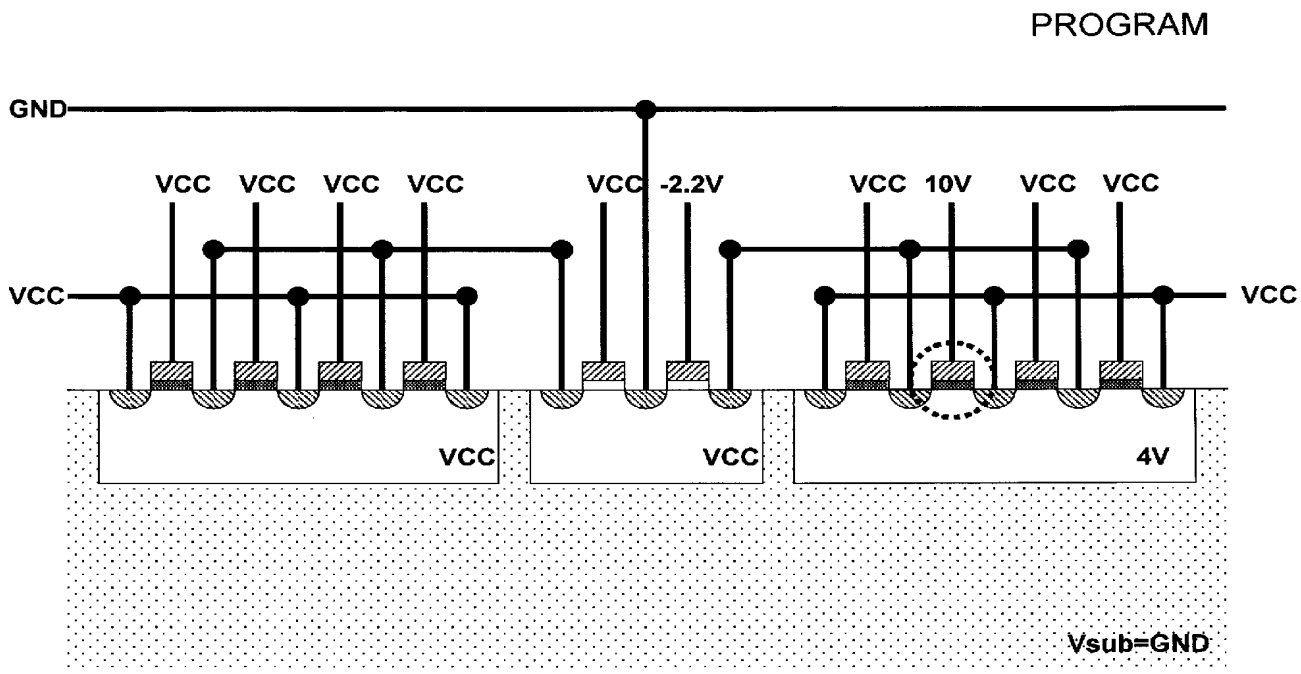
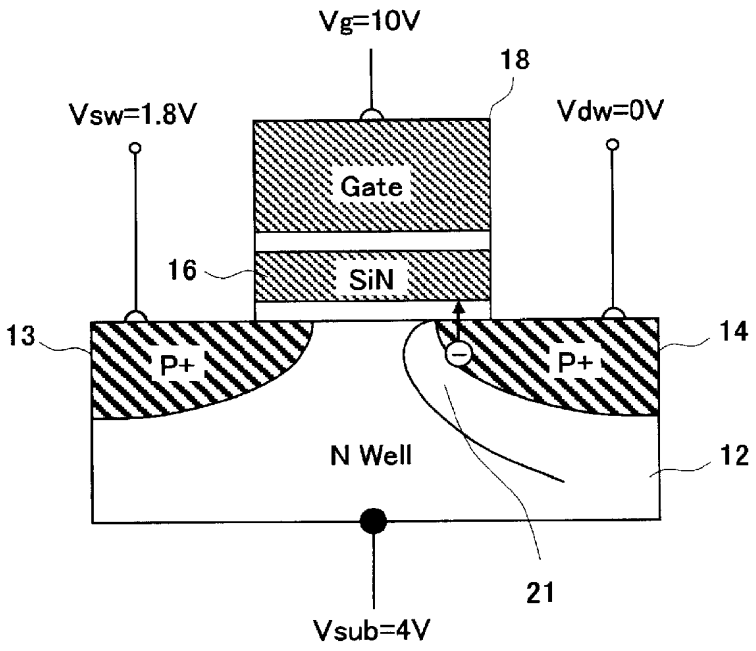

PROGRAM
GND
VCC VCC VCC VCC
VCC -2.2V
VCC 10V VCC VCC
VCC
VCC
VCC
VCC
4V
Vsub=GND

FIG.5

(A)


Vg=10V
18
Vsw=1.8V
Vdw=0V
Gate
16
SiN
13
P+
P+
14
N Well
12
21
Vsub=4V

(B)

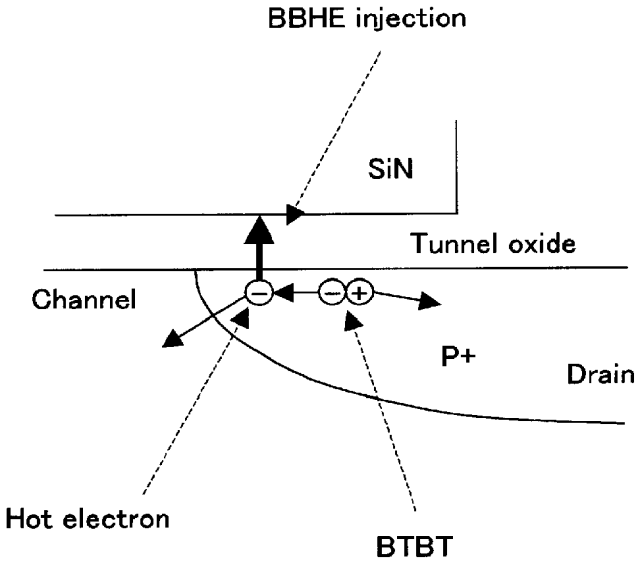

BBHE injection
SiN
Tunnel oxide
Channel
P+
Drain
Hot electron
BTBT

FIG.6

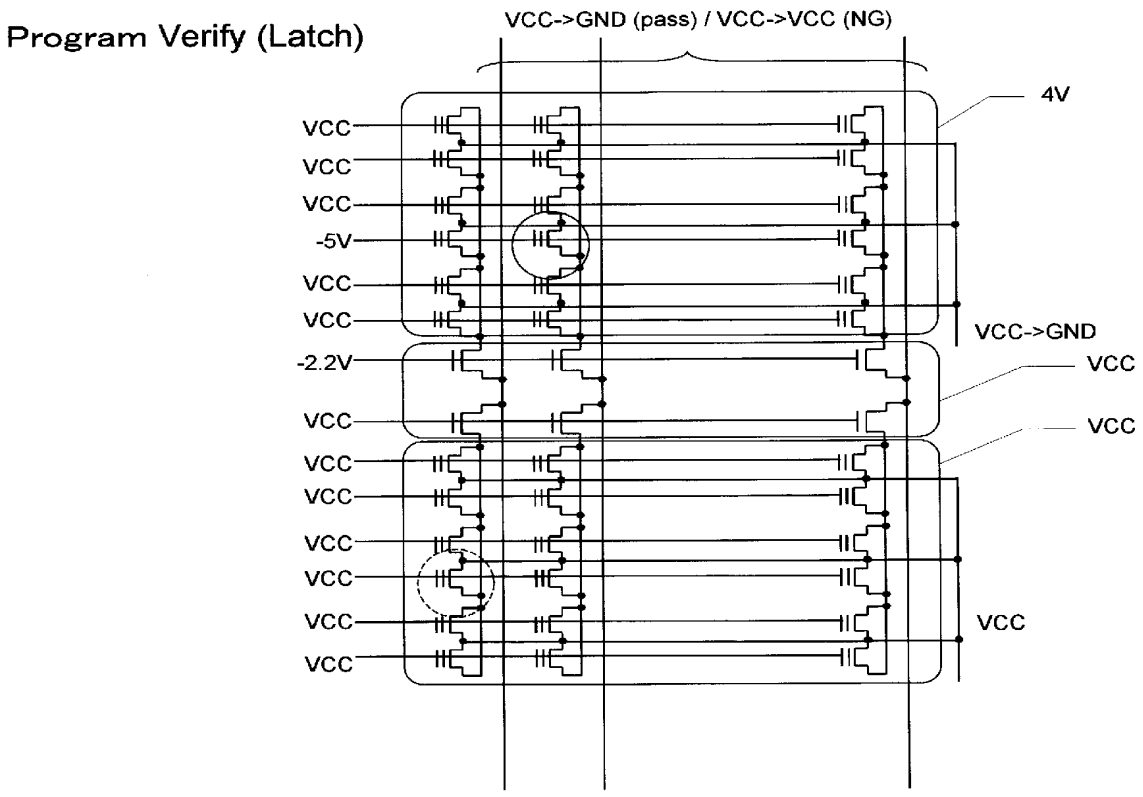

Program Verify (Latch)
VCC->GND (pass) / VCC->VCC (NG)
4V
VCC
VCC
VCC
-5V
VCC
VCC
-2.2V
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC->GND
VCC
VCC
VCC

FIG.7

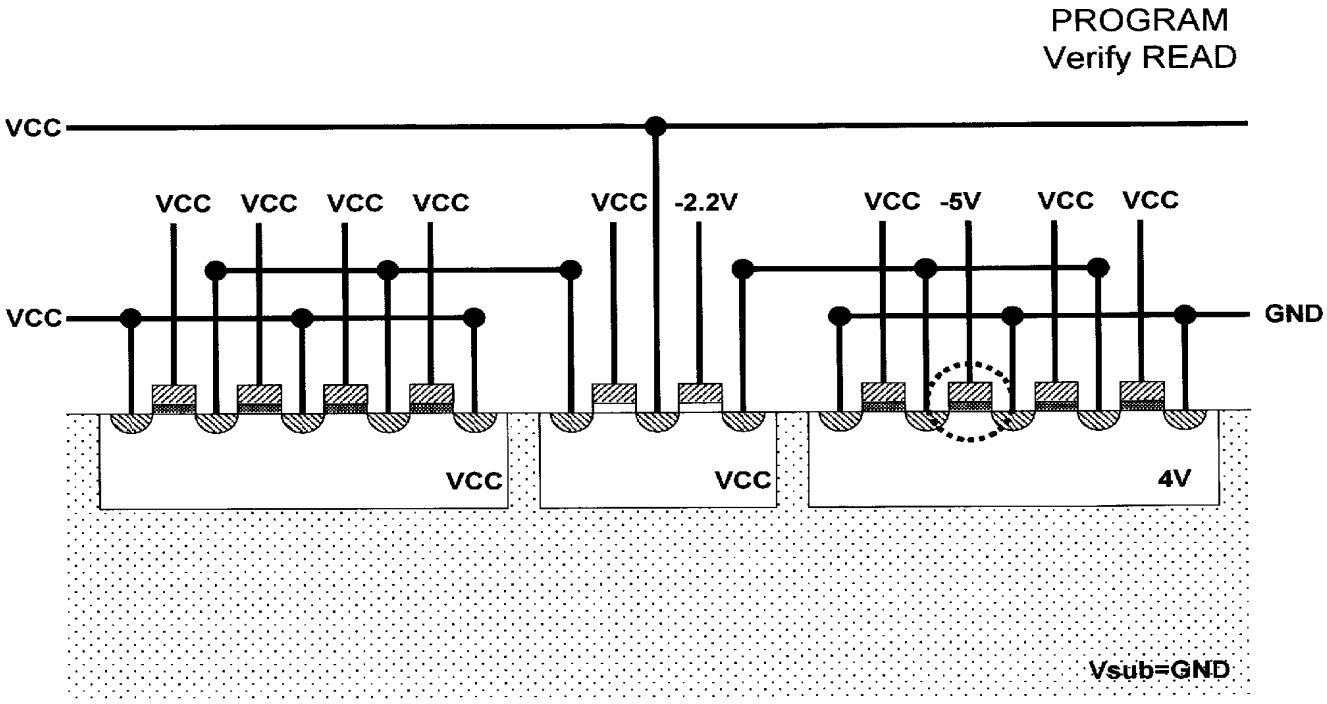

PROGRAM
Verify READ
VCC
VCC VCC VCC VCC
VCC -2.2V
VCC -5V VCC VCC
VCC
GND
VCC
VCC
4V
Vsub=GND

FIG.8

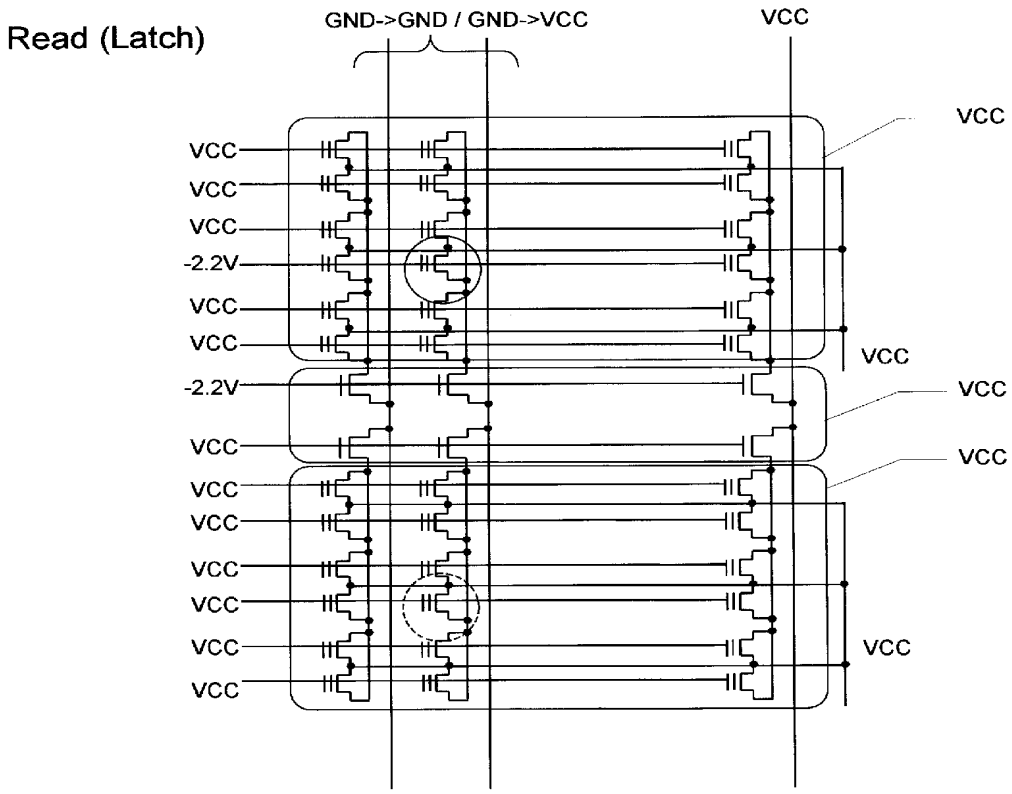

Read (Latch)
GND->GND / GND->VCC
VCC
VCC
VCC
VCC
VCC
-2.2V
VCC
VCC
VCC
-2.2V
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC

FIG.9

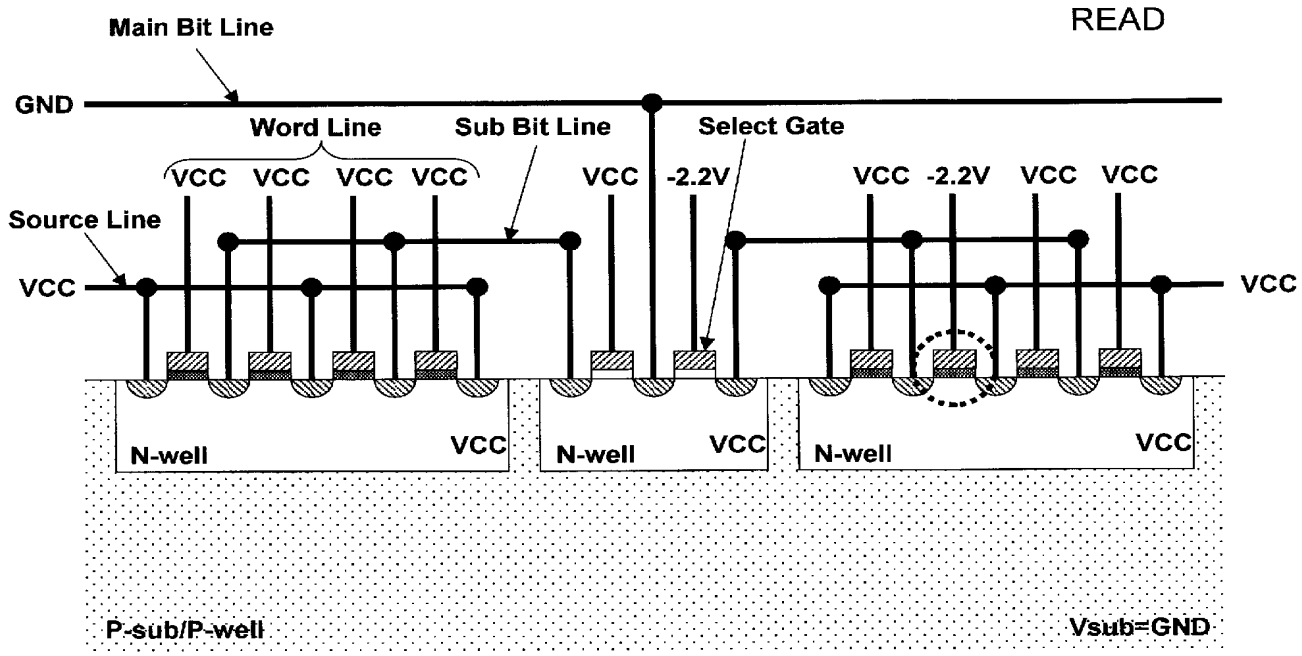

READ
Main Bit Line
GND
Word Line
Sub Bit Line
Select Gate
VCC VCC VCC VCC
VCC
-2.2V
VCC -2.2V VCC VCC
Source Line
VCC
VCC
N-well
VCC
N-well
VCC
N-well
VCC
P-sub/P-well
Vsub=GND

FIG.10

Erase (tunnel)

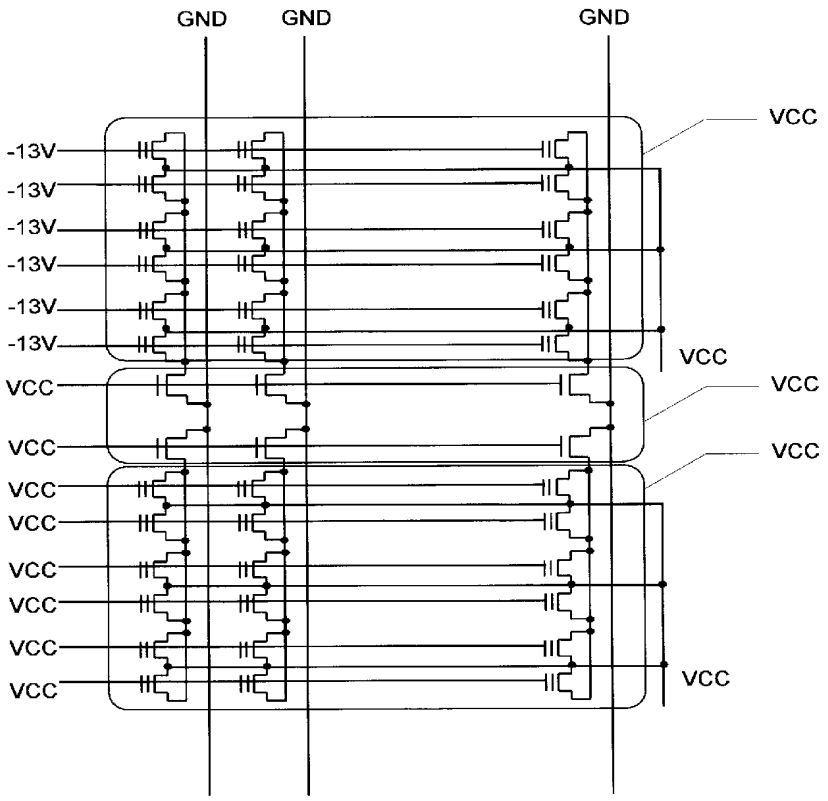


FIG.11

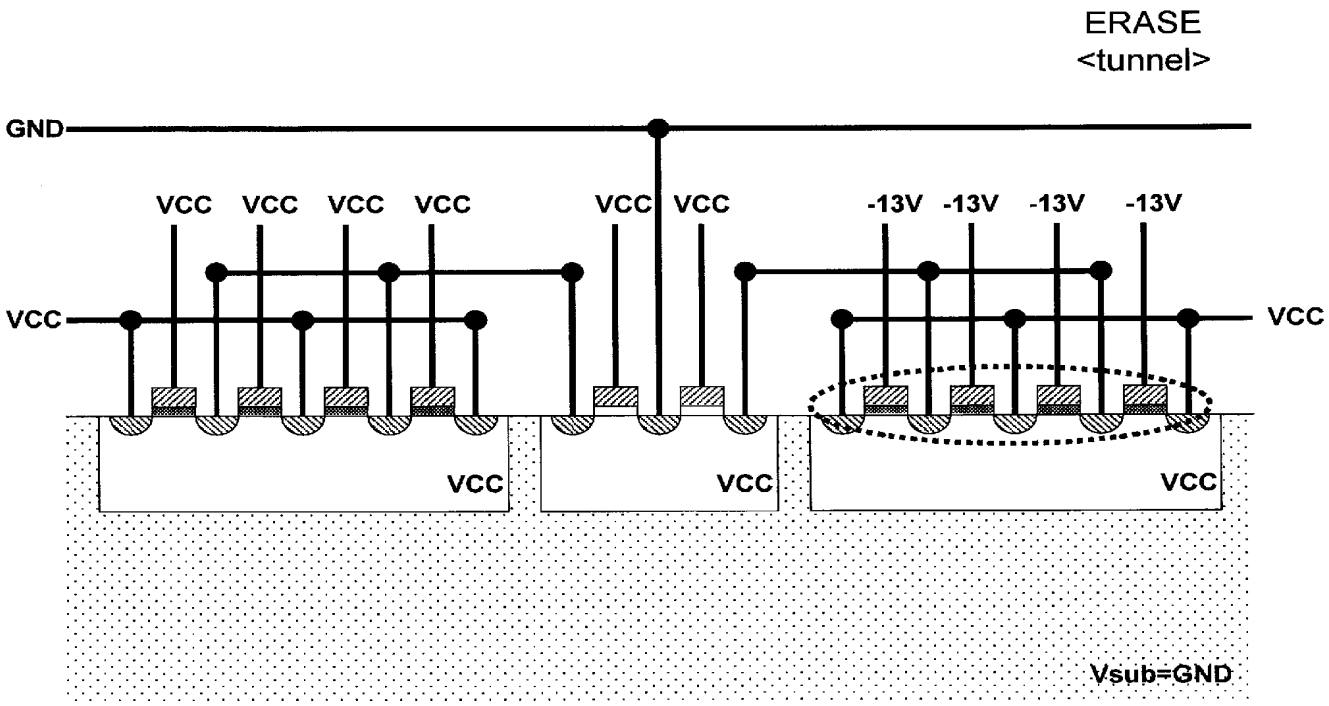

ERASE
<tunnel>
GND
VCC VCC VCC VCC
VCC VCC
-13V -13V -13V -13V
VCC
VCC
VCC
VCC
VCC
VCC
Vsub=GND

FIG.12

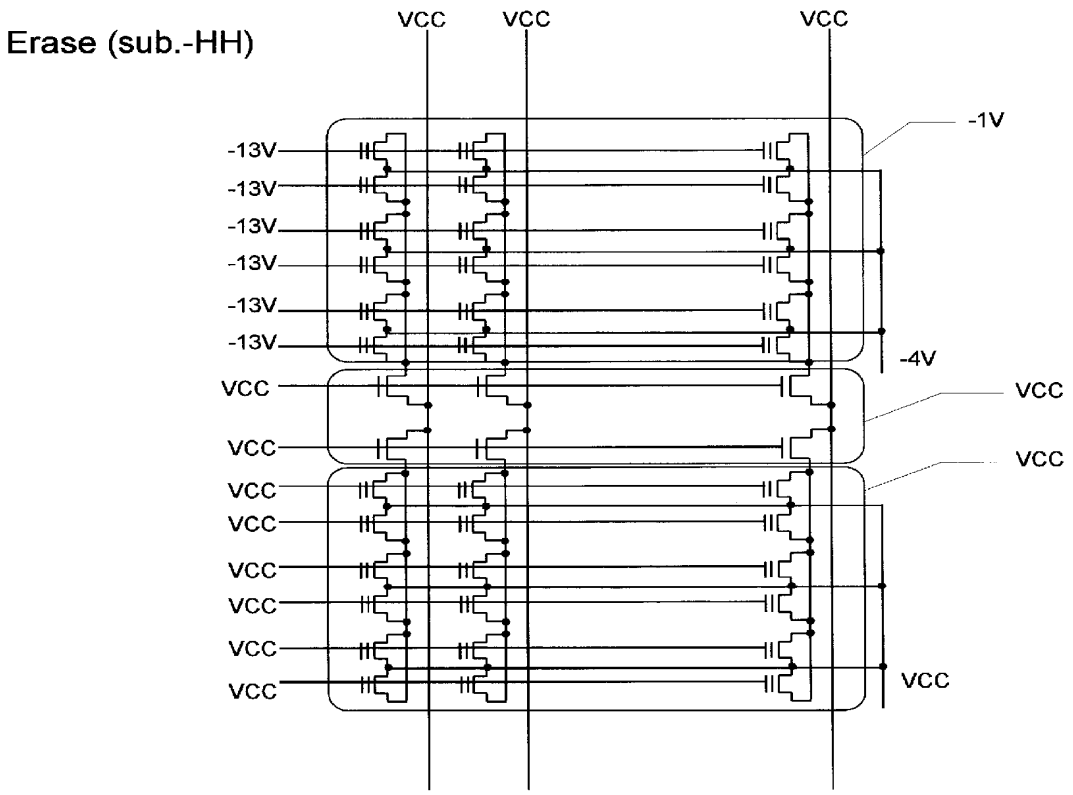

Erase (sub.-HH)
VCC
VCC
VCC
-1V
-13V
-13V
-13V
-13V
-13V
-13V
-4V
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC

FIG.13

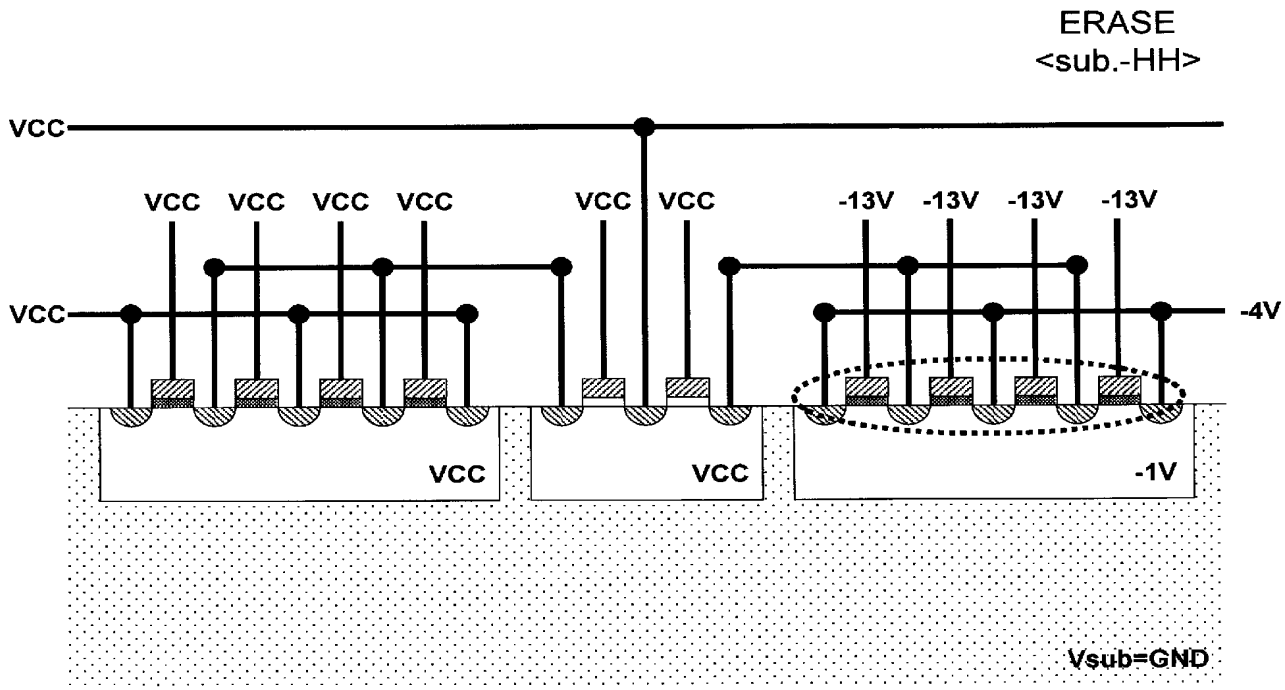

ERASE
<sub.-HH>
VCC
VCC VCC VCC VCC
VCC VCC
-13V -13V -13V -13V
VCC
-4V
VCC
VCC
-1V
Vsub=GND

FIG.14

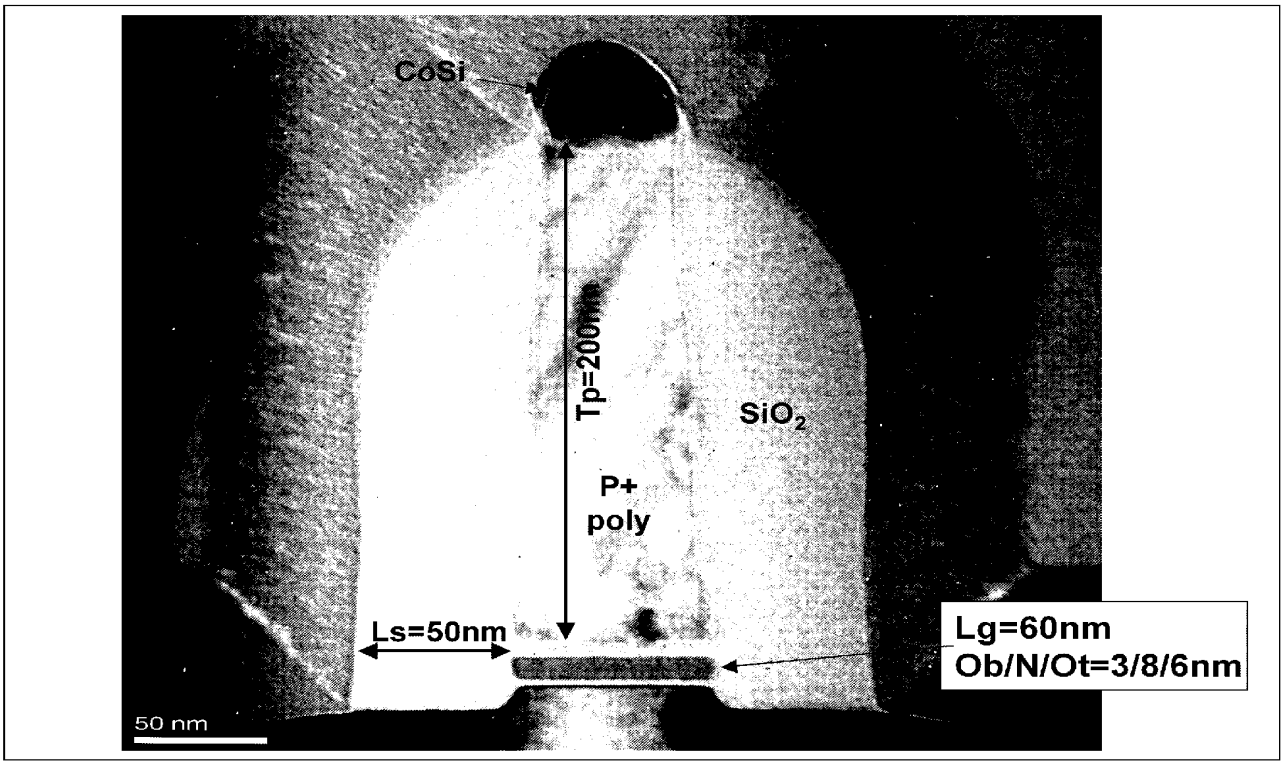


FIG.15

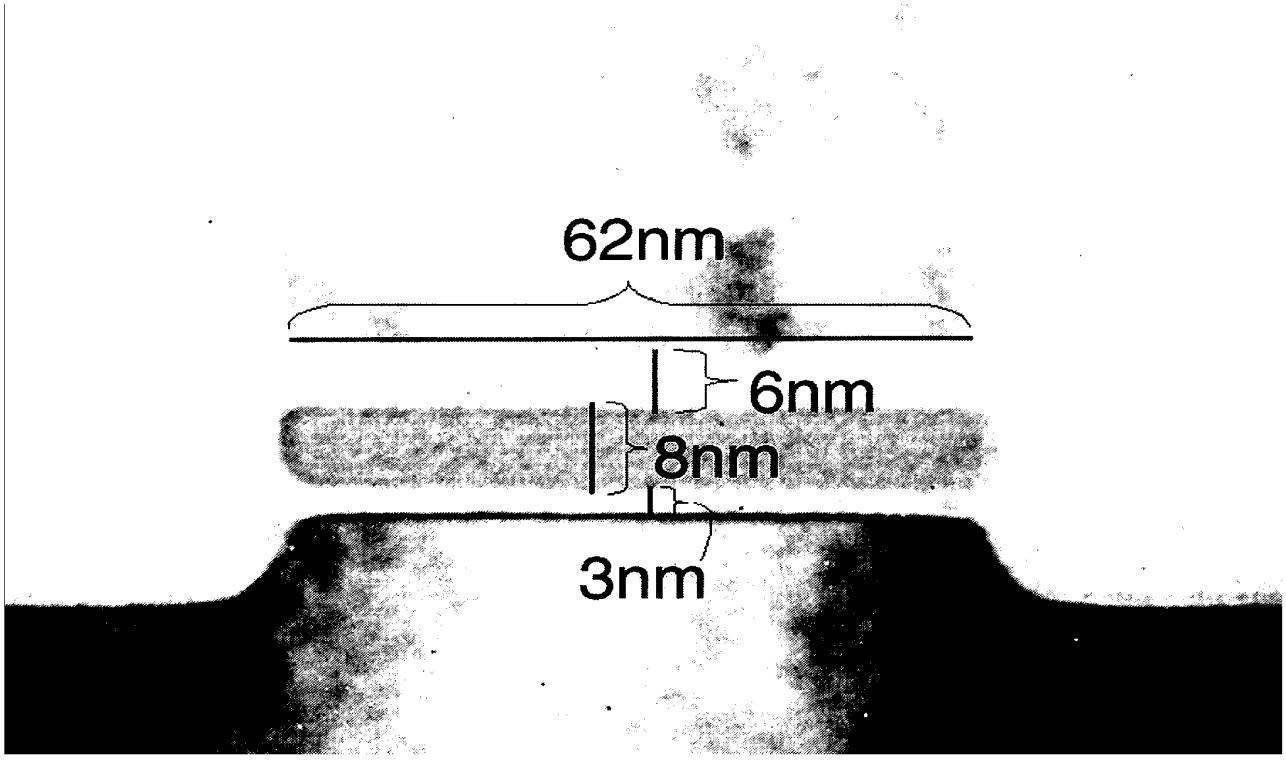


FIG.16

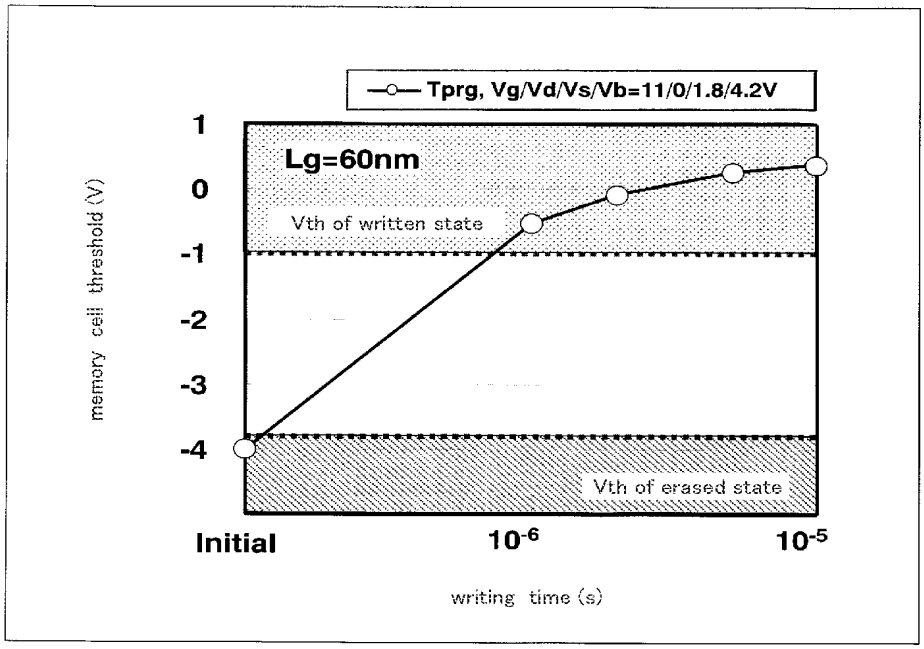

Tprg, Vg/Vd/Vs/Vb=11/0/1.8/4.2V
Lg=60nm
Vth of written state
Vth of erased state
1
0
-1
-2
-3
-4
memory cell threshold (V)
Initial
10-6
10-5
writing time (s)

FIG.17